AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (currently amended) A method of fabricating a MOSFET device, comprising:

forming a gate on a substrate, said gate comprising a gate dielectric layer and a conductive layer;

forming a liner on the sidewall of said gate;

performing a first-type ion implantation, using said gate and said liner as a mask, to form a source/drain region outside of said gate in the substrate;

etching said liner to reduce the lateral thickness of said liner on the sidewall of said gate; and

performing a second-type ion implantation, using said gate and the etched liner as a mask, to form a halo region surrounding said source/drain region.

2. (original) The method of claim 1, wherein said conductive layer comprises a polysilicon layer.

3. (original) The method of claim 2, wherein said conductive layer further comprises a silicide layer on said polysilicon layer.

4. (original) The method of claim 1, wherein forming said liner on the sidewall of said gate is performed by rapid thermal oxidation.

5. (original) The method of claim 1, wherein said first-type ions are N-type ions and said second-type ions are P-type ions.

6. (original) The method of claim 1, wherein said first-type ions are P-type ions and said second-type ions are N-type ions.

7. (original) The method of claim 1, wherein said gate further comprises a cap layer on said conductive layer.

8. (currently amended) A method of fabricating a MOSFET device, comprising:

forming a gate on a substrate, said gate comprising a gate dielectric layer and a conductive layer;

forming a liner on the sidewall of said gate;

performing a first-type ion implantation, using said gate and said liner as a mask, to form source/drain regions outside of said gate in the substrate;

etching said liner on one sidewall of said gate to reduce the lateral thickness of said liner; and

performing a second-type ion implantation, using said gate and the etched liner as a mask, to form a halo region surrounding one of said source/drain regions adjacent to the etching side.

9. (original) The method of claim 8, wherein said conductive layer comprises a polysilicon layer.

10. (original) The method of claim 9, wherein said conductive layer further comprises a silicide layer on said polysilicon layer.

11. (original) The method of claim 8, wherein said liner is formed on the sidewall of said gate by rapid thermal oxidation.

12. (original) The method of claim 8, wherein said first-type ions are N-type ions and said second-type ions are P-type ions.

13. (original) The method of claim 8, wherein said first-type ions are P-type ions and said second-type ions are N-type ions.

14. (original) The method of claim 8, wherein said gate further comprises a cap layer on said conductive layer.

15. (original) The method of claim 8, wherein said MOSFET device is used as an access transistor of a memory cell used in a memory, said source/drain region with said surrounding halo region is connected to a bit line.

16. (original) The method of claim 8, before etching said liner on one sidewall of said gate further comprising forming a mask layer covering another side of said gate.

17. (original) The method of claim 16, wherein said mask layer comprises a photoresist layer.